PLDBEITO Specification

Version	Note	Date
V1.0	Create	2019/05/29
V2.0	Modify Pin Define	2019/10/29
V2.2	Add 4.3	2020/02/25
V2.3	Add Section5,Section6	2020/08/14
V2.4		2020/12/28

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1.Functional Characteristics

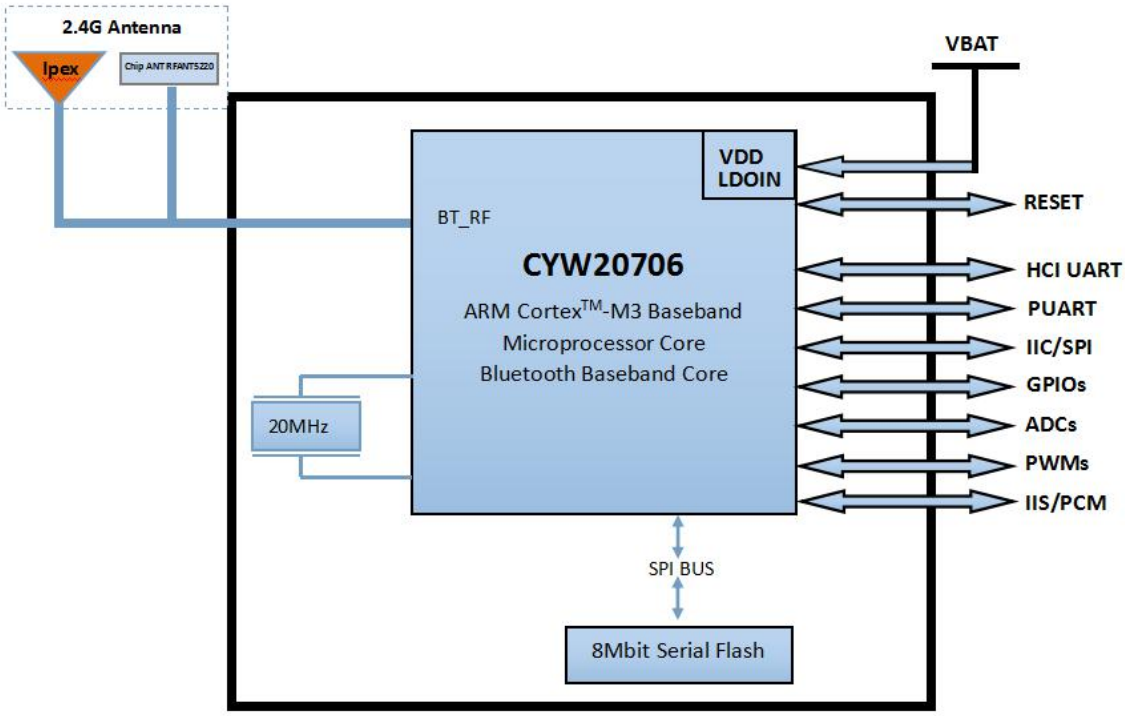
PLDBEITO is SOC module developed based on the Bluetooth 5 standards. the internal integration architecture ARM® Cortex®-M3 processor.It has the advantage of small volume, low power consumption, long distance transmission, strong anti-jamming capability, low cost.Specifically applied to Bluetooth low power control area,and suitable for various occasions short distance wireless communication.

The PLDBEITO is the optimal solution for voice, data, home automation, accessories and other applications that require a Bluetooth SIG standards-compliant interface. The PLDBEITO supports a host command interface (HCI) through USB or UART and also supports PCM audio. The PLDBEITO transceiver's enhanced radio performance meets the most stringent industrial temperature application requirements for compact integration into mobile handset and portable devices.

The module includes 20Mhz Crystal and 8Mb SPI flash.

Circuit block diagram of the module is shown in Figure 1.

Figure 1: PLDBEITO Circuit Block Diagram



1.1.Product Feature

1. PLDBEITO under Bluetooth 5 specification. including BR/EDR/BLE.
2. Supports A2DP, AVRCP, HSP, HFP, GATT, SPP, HIDD, HIDH, ANCS, AMS, IAP2, PBAP, OBEX, WeChat, HomeKit, Wide band speech (WBS)
3. Support Beacon function.
4. Support OTA Upgrade, UART Upgrade.
5. I2S/PCM for BT audio

1.2. Main Application Domain

1: Bluetooth Printer/Scanning device
2: Home automation / Intelligent access control system.
3: Industrial telemetry / Industrial data collection.
4: Bluetooth and RS232 (RS485) serial data transfer.

2.Electrical Specifications

- Integration architecture ARM® Cortex®-M3 processor
- 352KB RAM,848KB ROM,8Mbit Flash
- Include 8Mbit SPI FLASH, Memory size is optional
- Supports Cypress proprietary data rate up to 2 Mbps

2.1.Absolute Ratings

Parameter	*Specification*			*Unit*
	Min.	*Typical*	*Max.*	
Power Supply	-0.3	3.3	+3.8	V
Current Consumption	-	-	100	mA
Storage temperature	-40	-	+150	℃
Working temperature	-30	-	+105	℃
ESD HBM	-2K	-	+2K	V
ESD CDM	-500	-	+500	V
Latch-up	TBD	TBD	TBD	mA

2.2.Recommended Operating Conditions

Parameter	*Specification*			*Unit*
	Min.	*Typical*	*Max.*	
Power Supply	3.0	3.3	3.6	V

Digital I/O Characteristic(VDDIO=3.3V)

Characteristics	*Symbol*	*Specification*			*Unit*
		Min.	*Typical*	*Max.*	
Input Low Voltage	VIL	-	-	0.8	V
Input High Voltage	VIH	2.0	-	-	V
Output Low Voltage	VOL	-	-	0.4	V
Output High Voltage	VOH	VBAT-0.4V	-	-	V

2.3.Power Consumption

Current consumption measured in BLE mode with 3.30V power on in VBAT.

Operational Mode	*Conditions*	*Typical*	*Unit*
Receiving	Receive (1 Mbps) current level when receiving a basic rate packet	12.5	mA
Transmitting	Transmit (1 Mbps) current level when transmitting a basic rate packet.	26.5	mA
Flash Operation	Erase and write flash	60	mA
HIDOFF(Deep Sleep)		1.8	uA

Current consumption measured in Pairlink connected mesh mode.

Work Mode	*Status*	*Average*	*Unit*
Mesh disable	Power on	12.18	mA
Discoverable	Broadcast	18.84	mA
Single mode	Home id configurated	13.03	mA
Connected	IN MESHnet	14.62	mA

Note: These data are based on the development board with Demo_SW, only for customer reference. The actual power consumption according to the customer's application

2.4.RF Specifications

Parameter	*Conditions*	*Min.*	*Typical*[A]	*Max.*	*Unit*
Receiver RF Specifications					
Frequency range	-	2402	-	2480	MHz
RX sensitivity[B]	GFSK,0.1％BER,1Mbps	-	-93.5	-	dBm
	Π/4-DQPSK, 0.01％BER,2Mbps	-	-95.5	-	dBm
	8-DPSK, 0.01％BER,3Mbps	-	-89.5	-	dBm
Maximum input	GFSK,1 Mbps	-	-	-20	dBm
Transmitter RF Specifications(TBD)					
Frequency range	-	2402	-	2480	MHz
Class 1: GFSK TX power		-	12	-	dBm
Class 1: EDR TX power		-	9	-	dBm
Class 2: GFSK TX power		-	2	-	dBm
Power control step	-	2	4	8	dB

A.Typical operating conditions are 3.3V operating voltage and 25°C ambient temperature.
B.The receiver sensitivity is measured at BER of 0.1% on the device interface.

3.Physical Parameters

Parameter	*Performance*	*Note*
Distance	50M	Data Transfer (BLE) Environment: Sunny and open Airspeed: 1Mbps
	10M	AUDIO(BR/EDR) Environment: Sunny and open
Crystal	20MHz	Industry Standard
Protocol	Bluetooth 5	Including BR/EDR/BLE
Package	Patch	Refer to section 4.4
IC	CYW20706	49-ball FcBGA
RAM	352KB	Patch RAM(64KB)\Data RAM(288KB)
ROM	848KB	I-ROM(800KB)\D-ROM(48KB)
FLASH	8Mbit	
Core	ARM Cortex-M3	
Dimensions	16.8mm*11mm*2.6mm	L*W*H

3.1.Peripheral Interface

- 1 x I2S/PCM interface
- 1 x PUART interface with CTS/RTS
- 1 x HCI UART interface with CTS/RTS
- 1 x SPI interface with master/slave configurable
- 1 x I2C interface with master/slave configurable
- 12 x GPIO
- 11 x ADC input
- 4 x PWM interface

4.Hardware design and PCB layout

4.1.Pin assignment and Pin description[ab]

PLDBEITO Pin definition can refer to Figure 2.

Table 1:Module Pin Description

Pin Number	*Pin Name*	*I/O*	*POR State*	*Alternate Function Description*
10	VBAT	ADI	/	Power Supply
1,2,3,9,17, 18,26	GND	GND	/	Connect to Ground
11	RESET	DI		INPUT. Reset signal (active Low). Floating if not used
7	RECOVERY	I		SPI2 Master In Slave Out. For Test.
3	UART_RTS	I,PU		RTS for HCI UART interface. NC if unused.
4	UART_CTS	I,PU		CTS for HCI UART interface: NC if unused.
5	UART_RXD	I		Serial data input for the HCI UART interface.
6	UART_TXD	O,PU		Serial data input for the HCI UART interface.
8	P15/ADC_IN	DIO	Floating	GPIO:P15/ADC_IN
13	P30	DIO	Floating	GPIO:P30
14	P25	DIO	Floating	GPIO:P25/P32
15	P4/PUART_RX	DIO	Floating	GPIO:P4/P24 PUART_TX
16	P36	DIO	Floating	GPIO:P36/P38
19	P31/PUART_TX	DIO	Floating	GPIO:P31 PUART_RX
20	P34/I2S_WS	DIO	Floating	GPIO:P34 I2S_WS /PCM_SYNC
21	P12	DIO	Floating	GPIO:P12 I2S_DI/PCM_IN/I2C_SDA
22	P29/I2S_DATA	DIO	Floating	GPIO:P29 I2S_DO/PCM_OUT/I2C_SCL/PWM3
23	P28/I2S_SCLK	DIO	Floating	GPIO:P28 I2S_SCLK/PCM_CLK/PWM2
24	P26	DIO	Floating	GPIO:P26/P11

				PWM0
25	P27/I2S_MCLK	DIO	Floating	GPIO:P27/P33 I2S_MCLK/PWM1

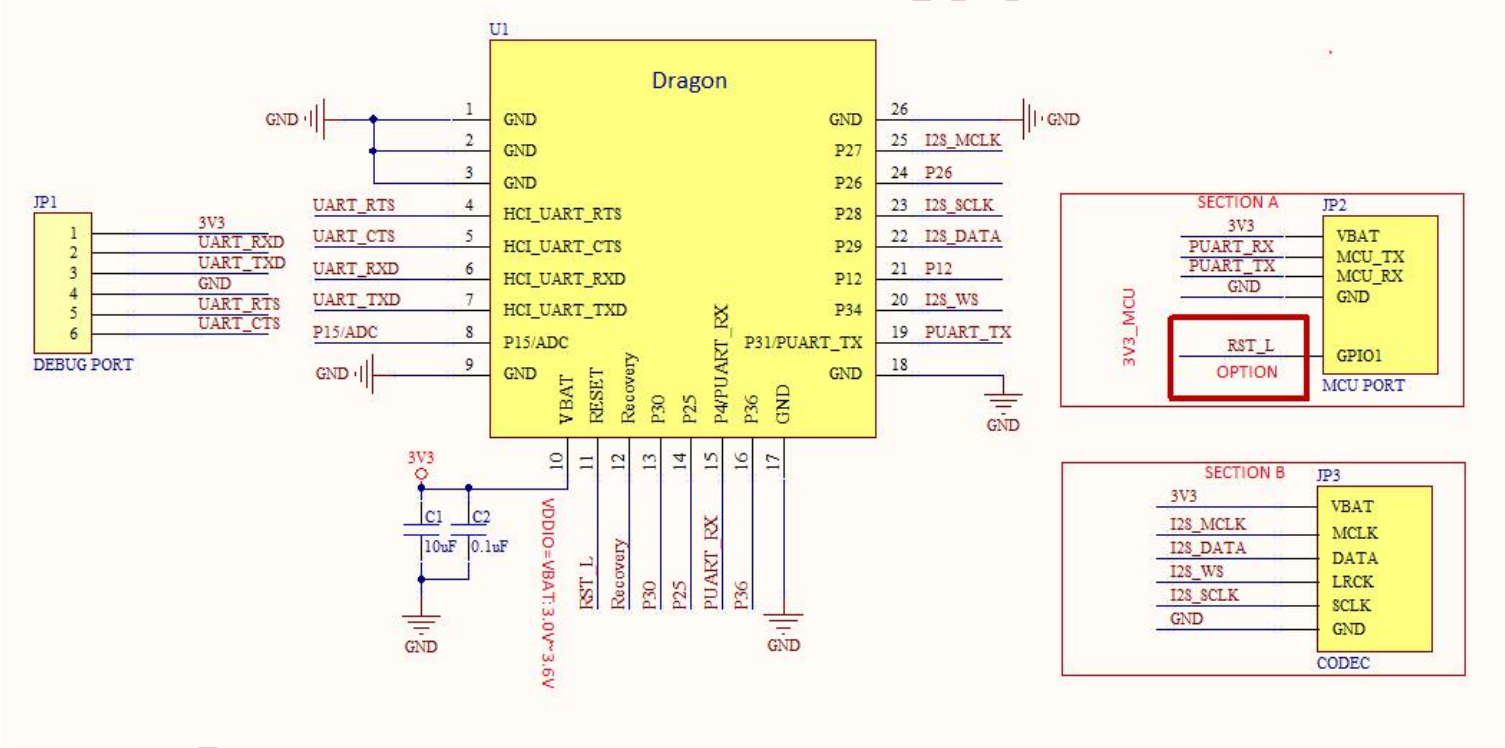
a. For more GPIO function configuration questions, contact to Pairlink.

b. During power-on reset, all inputs are disabled.

4.2.Reference Design

The latest schematic and design examples, bill of material, and layout file are available from original developer . Contact us for details.

Figure 2: Module Reference Design



Circuit Description

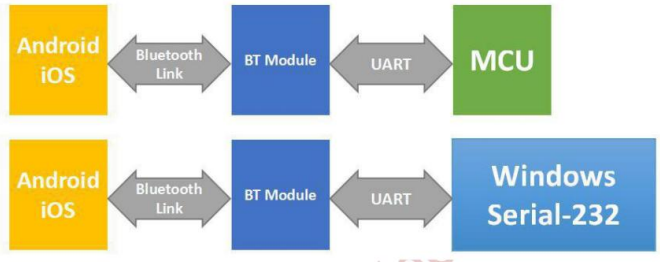
1:VBAT supply voltage value is 3.0V-3.60V.

2:PIN12(Recovery) reserved for testing.

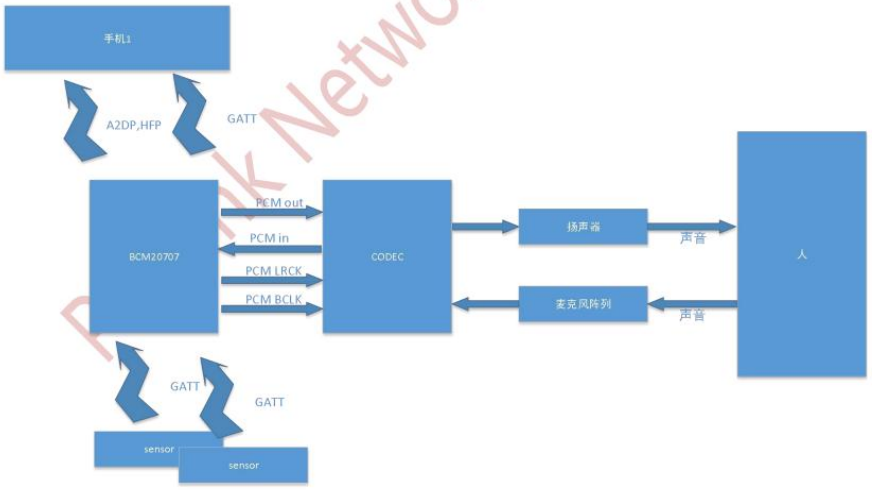
3:PIN11(RST_L) is Module Reset_Control (active Low) ,Keep floating if the user not use.

4:Reserve JP1 burning interface if the PCB board has enough space.

5:The application block diagram of SECTION A is shown below:



6:The application block diagram of SECTION B is shown below:



7:PLDBEITO not support GPIOs supermux,for more GPIO function configuration questions, contact the Pairlink.

4.3.Interface Signal Function Selection

PLDBEITO not support GPIOs Supermux. IIC\IIS\PWM\SPI\ADC can't be configured at the same time. If the customer wants to use all functions, it can be assigned by Pairlink.

Peripheral_UART			
P_UART_TX		P_UART_RX	
PIN Number	PIN Name	PIN Number	PIN Name
19	P31	15	P4

IIC			
IIC_SDA		IIC_SCL	
PIN Number	PIN Name	PIN Number	PIN Name
21	P12	22	P29

SPI							
SPI_CS (SLAVE)		SPI_CLK (Mater and Salve)		SPI_MOSI (Mater and Salve)		SPI_MISO (Mater and Salve)	
PIN Number	PIN Name	PIN Number	PIN Name	PIN Number	PIN Name	PIN Number	PIN Name
24	P26	16	P36	25	P27	14	P25

IIS							
I2S_WS		I2S_DATA		I2S_SCLK		I2S_MCLK	
PIN Number	PIN Name	PIN Number	PIN Name	PIN Number	PIN Name	PIN Number	PIN Name
20	P34	22	P29	23	P28	25	P27

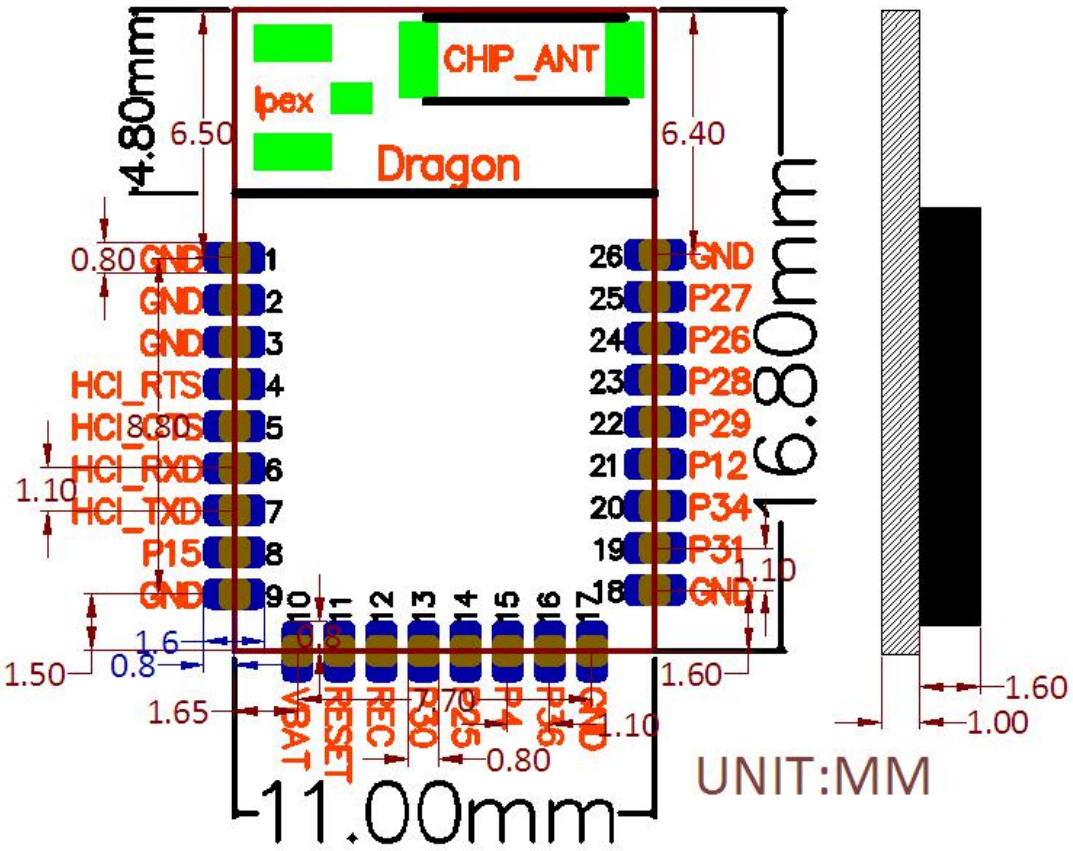
PWM							
PWM0		PWM1		PWM2		PWM3	
PIN Number	PIN Name	PIN Number	PIN Name	PIN Number	PIN Name	PIN Number	PIN Name
24	P26	25	P27	23	P28	22	P29

4.4.Appearance and Dimensions

Figure 3 shows the size of the module.The components and prominent structure are not allowed put in this size range(16.8mm*11.0mm*2.60mm).

The following land pattern size is recommended for user board design. However, user can modify it according PCB soldering conditions. Sufficient examination is necessary if use the modified land pattern.

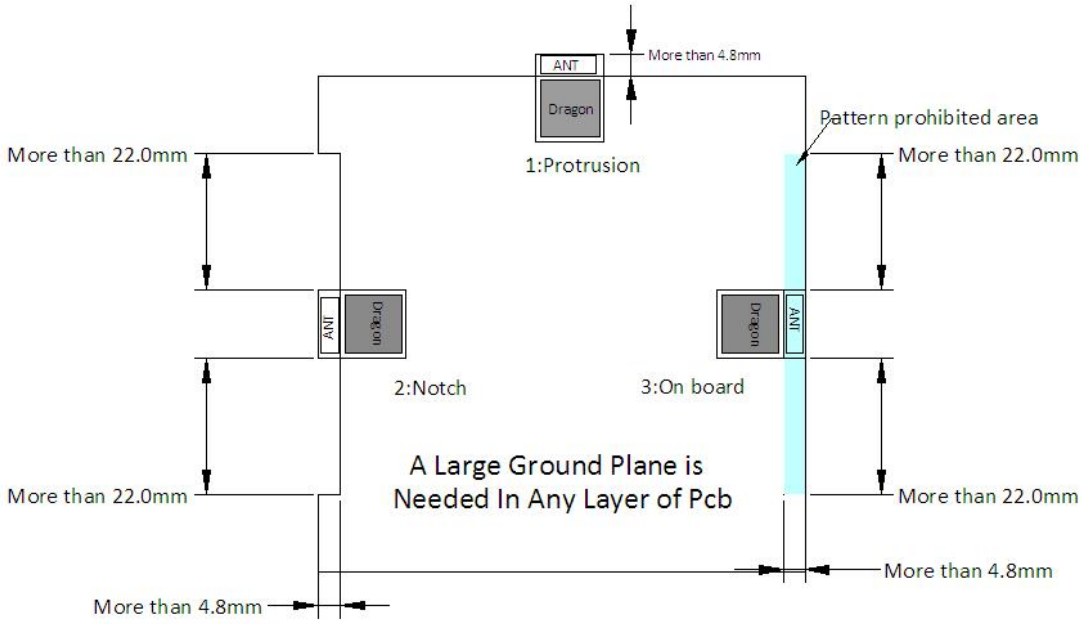
Figure 3: Mechanical Information



4.5.Module Layout Guideline

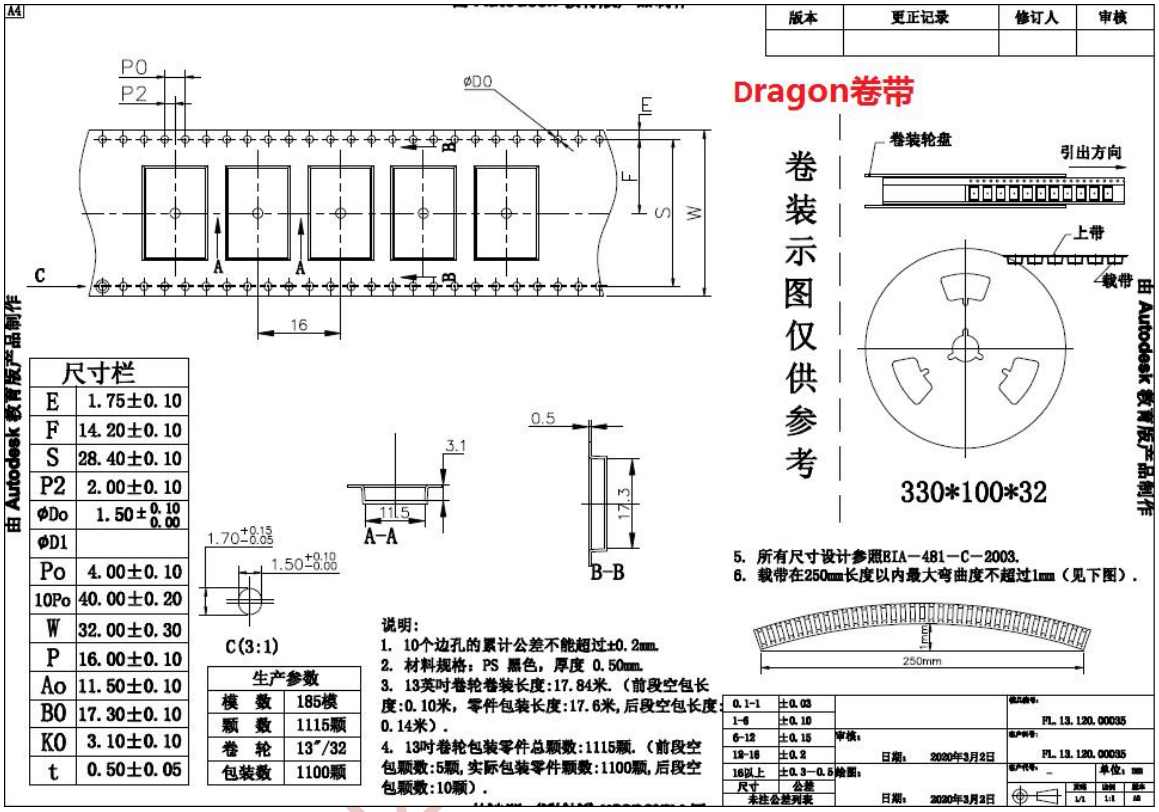
The layout on user PCB should be designed according to the following guideline.

Figure 4: Module Placement



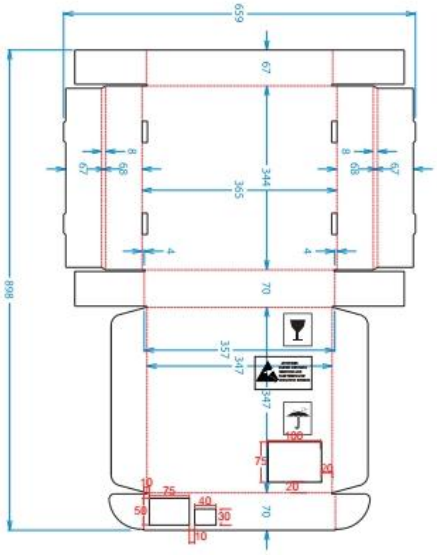
5.Packing Information

5.1.Rolling Information



Product name	MOQ	Packing method	Single package quantity
PLDBEITO	1100PCS	Tape and Reel	1100PCS

5.2.Master Carton Information



5.3.Label Information

A) Label on module

PLDBEITO has passed BQB\FCC\CE\IC\MIC\RoHS\SRRC certification

B) Label on vacuum bag and pizza box

Product name	PLDBEITO
Model name	Customer Corresponding Item Number
Customer PN	Customer Part Number
Quantity(PCS)	1100 pcs
Product date	YY.MM.DD
Product Version	SW Version
Product Type	Bluetooth Module
MFG PN	NA

C) Label on carton

Product Name	Customer Corresponding Item Number
Customer PN	Customer Part Number
Quantity(PCS)	5500pcs
Produced date	YY.MM.DD
C/N	Cartoon Number

6. Welding Declare

The PLDBEITO module only supports one reflow soldering , and the module failure caused by multiple reflow soldering is not responsible.

Figure 5: Standard Operation Procedure (SOP)